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System maximum power tracking among distributed power sources with series-output connected converters

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Abstract

Presented herein is a uniform input voltage distribution (UIVD) control (Siri, Truong, & Conner, 2005; Siri, Willhoff, & Conner, 2006; Siri & Willhaff, 2007; Siri, Willhoff, & Conner, 2007) for distributed-input series-output (DISO) converter power systems. The primary control objective of UIVD for DISO converters is to achieve grouped maximum power throughput from non-identical renewable power sources. Secondly, this paper features a revised maximum power tracking (MPT) controller design developed for DISO configurations that facilitate simultaneous processing of distributed power flows. Conventionally, the distributed source peak powers are individually tracked by converters that are controlled by independent MPT controllers without UIVD. However, when distributed power sources have similar peak power voltages with an achievable tracking efficiency of greater than 96%, such independent MPT controllers are not necessary. By utilizing UIVD control, near-maximum use of available power is achieved by using a single MPT controller. The resulting system and control architectures offer near-maximum power transfer with fewer number of parts used. Two DISO power converter bus architectures are described herein: one having a battery-dominated output voltage and the other with a regulated output voltage. Through computer simulation, both power architectures are validated for fault-tolerant grouped UIVD control.

Keywords: *power converter, maximum power tracking, series-output*

1. Introduction

Reliable and expandable power architectures and control approaches enable efficient power processing from distributed and unregulated power sources to a commonly usable and well-regulated voltage. The power systems using adopt distributed-input parallel-output (DIPO) converters are becoming a viable choice (Siri & Conner, 2001; Siri & Conner, 2002; Siri & Conner, 2003) for achieving reliable power/voltage performance in aerospace and renewable energy applications. Similarly, DISO converters can be controlled to achieve optimum power throughput from non-identical power sources by using UIVD control. This paper introduces the unconventional use of a single MPT controller combined with UIVD control developed for a DISO converter architecture, which simultaneously processes distributed flows of electricity with fault tolerance. Through modeling and simulation, this paper demonstrates that nearly full utilization of energy delivered by the distributed sources having non-identical peak power ratings can be achieved through a unified integration of MPT and UIVD control. Two power system architectures are studied in this paper; one is a battery-dominated bus, while the other is a regulated-voltage bus. Because of UIVD control, group maximum utilization of distributed power sources is accomplished by using one MPT controller rather than independent MPT controllers. Each of these controllers is conventionally dedicated to its respective power source.

Previous studies (Siri, Willhoff, & Conner, 2006; Siri & Willhoff, 2007; Siri, Willhaff, & Conner, 2007) of series-input parallel-output (SIPO) converter architectures revealed how UIVD control can achieve uniform power sharing among series-connected converters that absorb identical DC input currents. However, instead of power processing from a common power source, UIVD control adopted in SIPO converter architectures was designed (Siri & Sooksatra, 2011) to achieve optimum power throughput from series-connected power sources. Because different peak powers exist

among non-identical power sources, near- maximum utilization of all the power sources is still achievable by applying UIVD control as long as the peak power voltages of the individual sources are similar or mismatched within an acceptable tolerance (such as ± 20%), accordingly. UIVD serves as a cost-effective method of power management and distribution for SIPO converters having similar peak-power voltages.

Earlier studies (Siri & Conner, 2001; Siri & Conner, 2002; Siri & Conner, 2003; Siri & Sooksatra, 2014) of DIPO converter architectures also demonstrated the feasibility of using independent maximum power tracking (IMPT) controllers dedicated to each respective converter for regulating power flow from each distributed source without UIVD. The peak power delivered from each of the distributed power sources is independently tracked by the respective converter that is controlled by the respective independent MPT controller. However, when distributed power sources have similar peak power voltages and a tracking efficiency of at least 96% is expected, independent MPT controllers may not be necessary. Demonstrated herein is a single MPT controller, which was previously studied through modeling and simulation with SIPO converter architectures (Siri & Sooksatra, 2011) for tracking a system's optimum power point using DISO converters with UIVD control to support optimum power flows from distributed power sources. Each distributed power source is independently connected across the input port of its respective converter. For non-identical power sources, the unified MPT/UIVD system controller enables optimum power transfer from distributed power sources over uniform power sharing among DISO converters. The DISO converter architecture combined with UIVD and group MPT controller can tolerate multiple short-circuit faults across converter inputs. Furthermore, the revised MPT controller design is less complex than those MPT controllers used in the previous studies (Siri & Conner, 2001; Siri & Conner, 2002; Siri & Conner, 2003). Introduced herein is a novel system controller that offers regulation of the distributed input voltages using Maximum-Limit (ML) voltage feedback together with UIVD control to regulate the distributed source voltages at a system optimum-power voltage regardless of induced short-circuit faults. During fault conditions, the system optimum-power voltage is controlled for the remaining functional sources from which the total source power is kept as close as practical to the summation of the remaining functional ideal peak powers.

2. Converter power system description

Figure 1 depicts an output-isolated DC-DC converter with an opto-coupler circuit that provides electrical isolation for controlling the converter power flow using the control input (V_{Ci}). In this manner, many isolated-control converters can have their input power ports individually connected to their respective power sources, while the converters are independently controllable through their respective control inputs (V_{Ci}) and their outputs are connected in parallel for power delivery to a shared load. In general, each converter's input-power return (-IN) and the system controller's reference ground may not have the same operating voltage or are not the same electrical node. Therefore, isolated-control converters with their respective opto-coupler circuits provide flexibilities for interconnection among many converters such that their input power returns do not need to be tied together to the system controller's reference ground. Typically, an input-filter capacitor (C_{IN}) of sufficient capacitance is terminated across each converter input to achieve an acceptable AC input-ripple voltage, particularly, when the converter input voltage is controlled to meet certain control objectives.

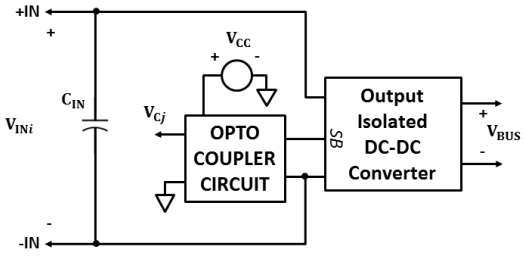

Figure 1 Basic DC-DC converter with an opto-isolated control input V_{Ci} that is electrically isolated from the converter's input power and return terminals

Each isolated-control DC-DC converter shown in Figure 1 can be a single-converter power stage or a group of multiple-converter power stages that are connected in parallel. These parallel-connected converter power stages of a current-mode type are preferred. The current-mode converter power stages allow for a common shared-bus voltage signal to command these converter power stages in unison to achieve uniform current-sharing and at the

same time to serve other control objectives. Different approaches of shared-bus current-sharing were studied for parallel-connected converters of current-mode type (Siri, 1999) and for those of non-current-mode type (Jordan, 1991-1996). According to these studies, some current-sharing control schemes are not able to realize the commonly controllable current-sharing shared-bus such as the scheme published by Jordan (1991-1996) since the parallel-connected converter power stages are not of the current-mode type, and its shared-bus can only be used for current-sharing purposes and cannot be controlled directly to serve other control objectives.

2.1 Battery-dominated power system

Figure 2 illustrates a DISO converter power system architecture consisting of three distributed-input converters with their outputs being series-connected across a battery bank having an output voltage VBUS. A system load may be terminated across the output voltage that becomes a battery-dominated voltage bus. Each of these three isolated-control dc-dc converters shares the following attributes: (a) includes a shared-bus control input (SB_i), which allows an external signal to take control of the converter power stage; (b) may represent a number of parallel-connected converter modules configured with shared-bus control inputs tied together to form a common shared-bus control port so as to achieve nearly uniform current-sharing; (c) may operate in a standalone configuration wherein the output is regulated at a pre-determined voltage and its shared-bus input is left unconnected; and (d) must provide electrical isolation between input and output. There are six feedback input signals feeding the system controller shown in Figure 2: the battery-bus voltage V_{BUS}, the system bus current I_{BUS}, the charging battery-bank current I_{BAT}, and the distributed input voltages V1, V2, and V3 of the three independently sourced converters. Figure 3 depicts a conceptual block diagram of the system controller employed in the battery-dominated power architecture shown in Figure 2. The system controller provides four basic control functions: (1) system battery charge control, (2) system distributed input-voltage regulation, (3) uniform input voltage distribution (UIVD), and (4) system maximum power tracking (MPT). The DISO converter system may include a bus stabilizer network terminated across the system output V_{BUS} located as close to the system output port as possible to damp out ac energy, thus ensuring system stability.

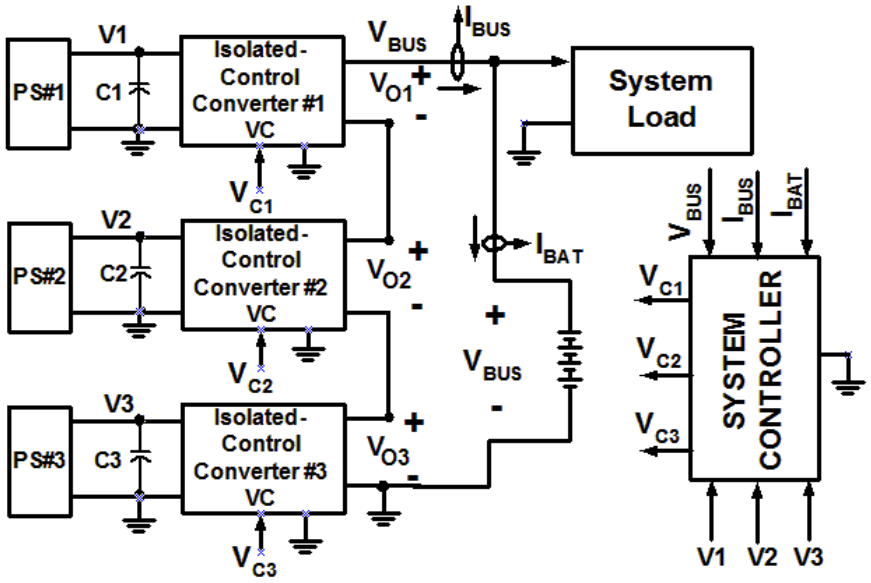

Figure 2 Battery-dominated 3-converter DISO power system with 3 distributed power sources

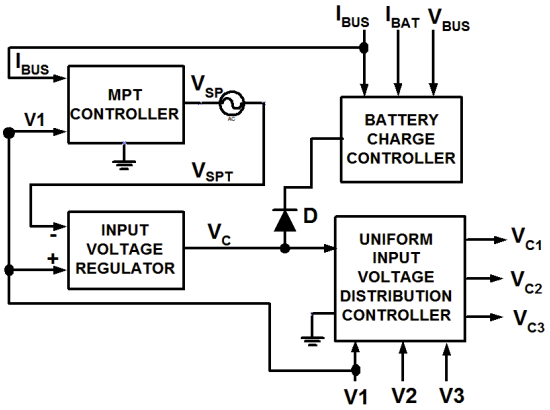

Figure 3 DISO converter power system UIVD controller

Typically, the battery charge controller shown in Figure 3 regulates the battery-bank voltage V_{BUS} to a preset value in accordance with its voltage-temperature (V/T) profile to prevent battery over-charging. When the battery-bank voltage V_{BUS} is below its preset value that is pre-assigned as a function of temperature, the battery-bank current I_{BAT} is regulated at a preset charge-current set-point determined by the charge controller. Active battery regulation of either its voltage ($V_{BUS)}$ or charge current (I_{BAT}) leads to a forward-voltage bias across the pull-down diode (D) shown in Figure 3. However, when V_{BUS}'s voltage and I_{BAT}'s current are respectively below the preset voltage value and the preset charge-current set-point, the system controller regulates the system distributed-input voltage, V1, at the optimum peak-power voltage that is determined by the MPT control. As long as the operating battery-bank voltage and current are below their preset voltage/charge-current values, the DISO converter power system is controlled to have an optimum power transfer from all distributed power sources by utilizing only one MPT controller that dominates its control over the battery charge controller through the primary control signal (V_C) and the reverse-biased diode (D). Only one of the following three operational modes is active at a time - battery voltage regulation mode for compliance with a V/T profile, battery charge-current regulation mode for serving a commanding charge rate, or distributed-input voltage regulation mode for tracking a system optimum-power voltage. During any of these three operating modes, converter-input voltages across the distributed power sources are always regulated to be equal by the UIVD controller that properly distributes three control voltage signals V_{C1}, V_{C2}, and V_{C3} to their respective isolated-control converters #1, #2, and #3.

In general, a DISO power system may consist of *N* isolated-control DC-DC converters with their respective *N* series-connected power sources PS#1, PS#2, . . . , and PS#*N*. During either the battery voltage/current regulation or the distributed-input voltage regulation, the converter-input voltage distribution controller as shown in Figure 4 produces secondary control signals (V_{d1}, V_{d2}, . . . , and V_{dN}). The secondary control signals are subtracted from the primary control voltage, V_C, to create a modified control voltages (V_{C1}, V_{C2}, . . . , and V_{CN}), each of which regulates its respective converter to accomplish uniform input voltage distribution.

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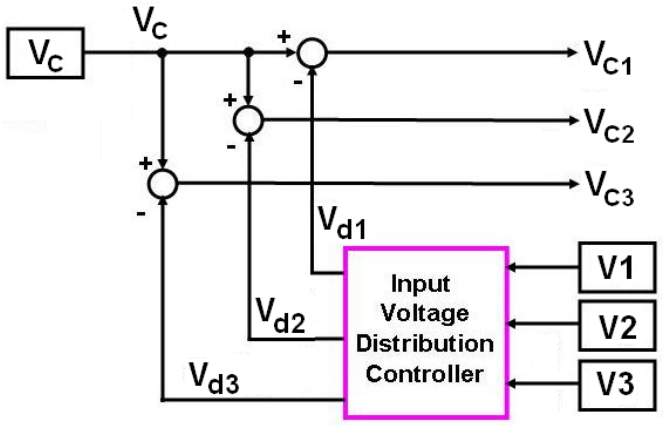

Figure 4 Uniform input voltage distribution controller block diagram for 3 DISO converters

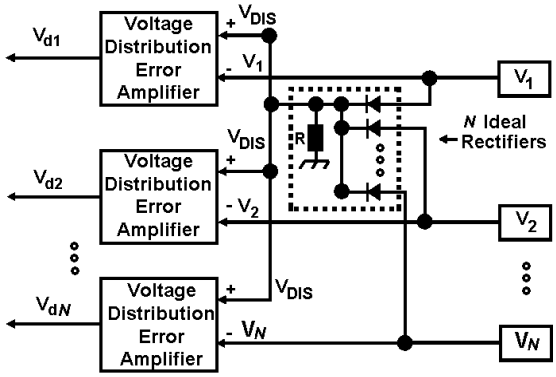

Figure 5 Fault-tolerant uniform input voltage distribution controller using the maximum-limit distribution reference

Figure 5 shows the UIVD controller that is based on the Maximum-Limit (ML) distribution reference, V_{DIS} = MAX(V_1, V_2, . . . , and V_N). To achieve fault-tolerance, a set of ideal rectifiers is included as part of the UIVD controller to produce a common distributed voltage reference signal, V_{DIS}, which is the highest output voltage obtained from one of the converters within the power system. Therefore, if a converter fails with its input short circuited, V_{DIS} is automatically updated to compensate for the loss of a failed converter or the failure of its respective input power source. For the system to tolerate at least one converter input short-circuit failure, two ideal rectifiers are required to sense two input voltages obtained from two converters. Up to *N* ideal rectifiers are included in the UIVD controller for an *N*-converter DISO system.

Consequently, Figure 5 illustrates the UIVD control for an *N*-converter DISO power system with fault-tolerance. A common distributed voltage reference signal (V_{DIS}) is derived from *N* cathode-parallel-connected ideal rectifiers so as to individually sense the input voltages of converters #1, #2, . . . , and #*N*. If one converter fails to build up its input voltage, the *N*-1 remaining converters will be controlled to have uniform input voltage distribution. A protection fuse which can be inserted in series with either the positive input of each DISO converter or the positive output of its respective power source provides a simple method of fault clearing which prevents thermal overstress from happening to the power system.

The DC gain for each voltage distribution error amplifier shown in Figure 5 does not need to be high in order to achieve uniform input voltage

distribution. On the contrary, high DC gain within each distribution error amplifier causes the converter-input voltage distribution controller to dominate the battery charge control and the distributed-input voltage regulation modes of operation, resulting in insufficient charging to the battery bank.

2.2 Regulated-bus power system

Figure 6 shows another DISO converter power system architecture consisting of three independently sourced input converters with their outputs that are series-connected across a battery bank having an output voltage V_{BUS}. A system load may be terminated across the battery voltage V_{BUS} which serves as a battery-dominated voltage bus. Each of these three isolated-control dc-dc converters share the same four attributes previously described for Figure 2. There are seven feedback input signals feeding the system controller shown in Figure 6: the battery-bus voltage V_{BUS}, the regulated-bus output voltage V_{OUT}, the system battery-bus current (I_{BUS}), the charging battery-bank current (I_{BAT}), and the distributed input voltages V1, V2, and V3 of the distributed-input converters. Figure 7 depicts a conceptual block diagram of the system controller employed in the dual-bus power architecture shown in Figure 6. The system controller provides five basic control functions: (1) system output voltage regulation of V_{OUT}, (2) system battery charge control, (3) input voltage regulation of the distributed input voltages V1, V2, and V3, (4) uniform input voltage distribution (UIVD), and (5) system maximum power tracking (MPT). In the same manner, a bus stabilizer network may be terminated across the system output V_{OUT} located as close to the system output port as possible to damp out *ac* energy, thus ensuring system stability. The system regulated-bus voltage V_{OUT} is closed-loop controlled by an output-isolated DC-DC converter with its output port V_{O4} that is series-connected with the battery-bus voltage V_{BUS}. This special output-series-connected converter significantly improves the system efficiency since the converter output voltage V_{O4} can be a minor portion of the overall output voltage V_{OUT}, and the battery voltage V_{BUS} can be the major portion. The control signal V_{C4} drives the converter's power stage to regulate the V_{OUT}'s voltage at a fixed value above the system battery-bus voltage V_{BUS}. The system controller shown in Figure 7 provides a much more fault-tolerant coverage than the system controller shown in Figure 3 since the input voltage regulator controller has the distribution voltage V_{DIS} as its feedback input instead of the PS#1's voltage V1. Since V_{DIS} is the maximum-limit voltage that is the maximum voltage detected from those of the three power sources or V_{DIS} = MAX (V1, V2, and V3), the input voltage regulator provides active control on V_{DIS} to follow the commanding set-point voltage V_{SPT}. There always exists one converter's input voltage that is the highest among all the distributed-input voltages while they are controlled to have a uniform distribution at all times. This maximum-limit input voltage regulation allows the converter power system to tolerate more than one failure due to the short-circuit or open-circuit of power sources and/or short-circuit or overload across distributed inputs of DISO converters.

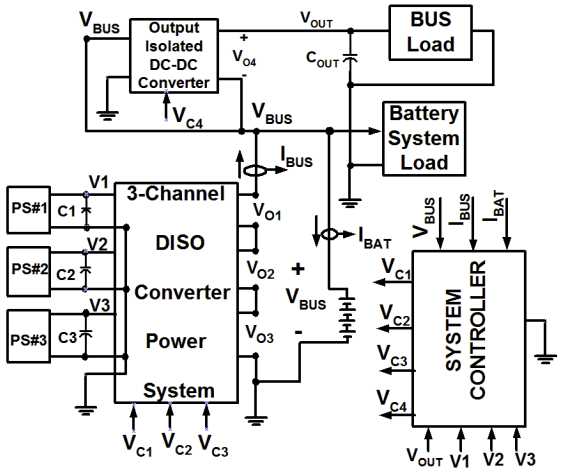

Figure 6 Dual-regulated bus power architecture with UIVD control

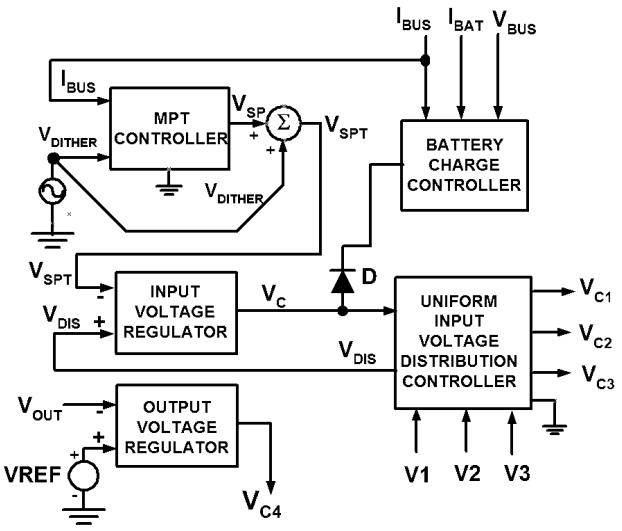

Figure 7 System controller for the dual regulated buses employed in the system shown in Figure 6

3. Simulation of DISO power systems

3.1 Battery-dominated power system simulation

A PSPICE model of the battery-dominated bus power system with three DISO converters and three distributed power sources, as shown in Figure 2, was developed and simulated to verify the basic functionality of each control loop. To verify the fundamental control behavior, the MPT control is enabled, and a solar array set-point voltage (V_{SPT}) is autonomously updated by the MPT controller to command the input-voltage regulation control loop to regulate the distributed sourcing voltages (V1, V2, and V3) at the system optimum power point voltage.

Figure 8 shows the simulation result that demonstrates a mode transition from the input-voltage regulation mode to the normal battery-charge current regulation mode, in which the charge-current set-point reference is reduced from far above 12 A to about 9.8 A at around time t = 5.04 s. This change of the set-point reference command causes the battery current to drop from 11.3 A to 9.8 A (on the lower plot of Figure 8), and the distributed sourcing voltages V1, V2, and V3, to increase from 32.24 V to 44.4 V (on the upper plot of Figure 8). During both modes of operation in steady state and their transient mode transitions, the three distributed sourcing voltages across the individual inputs of three respective converters are controlled to have uniform distribution at all times, as shown in three overlapping traces on the upper plot. The MPT controller is active during the input-voltage regulation mode; thereby, all the sourcing voltages contain a 20-Hz sinusoidal voltage V_{DITHER} that provides a continuous perturbation to all sourcing voltages and subsequently produces a 20-Hz response that is superimposed on the total bus current I_{BUS}. The 20-Hz frequency component within I_{BUS} is then extracted and processed by the MPT controller to update the system optimum peak-power commanding voltage V_{SP}. V_{SPT}, which consists of V_{SP} and a small-amplitude dither signal $V_{DITHER,}$ serves as the commanding voltage signal for regulation of the feedback voltage (V_{DIS}). V_{DIS} is the maximum-limit distribution reference as shown in Figure 5.

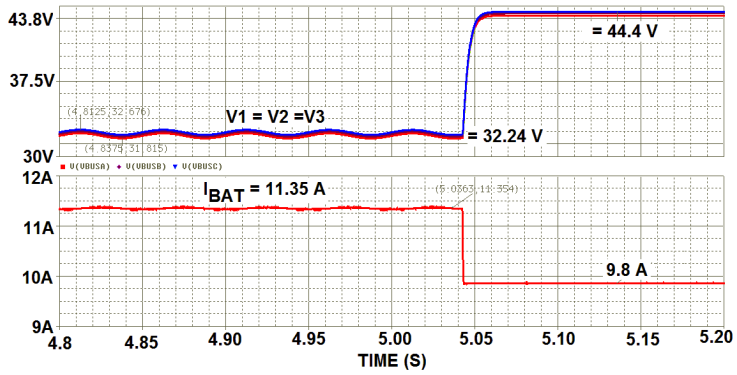

Figure 8 Simulated response of the three-converter DISO power system shown in Figure 2 during both input voltage regulation with UIVD and battery-charge current regulation modes of operation and their transient transition

Figure 9 illustrates another PSPICE simulation result that uncovers a transition from the battery charge current regulation mode to the input voltage regulation mode in which the three sourcing input voltages shown in the top plot are all regulated at the commanding set-point voltage V_{SPT} that is autonomously updated to approach a voltage corresponding to the system peak power voltage of 32.5 V (and eventually to 32.24 V) with 0.5 V peak-to-peak dither voltage ripple. This change in the operation mode occurs as a result of a step-change in the commanding charge-current reference signal from 0.1 V (corresponding to nearly 10-A charge-current) to 0.5 V (corresponding to 50-A charge current). This increased charger command causes diode D shown in Figure 3 to be reverse-biased since the input-voltage regulation controller has entered its active linear region to prevent the system input voltages V1, V2, and V3 from being collapsed below that corresponding to their existing commanding set-point voltage V_{SPT}. Consequently, the maximum power tracking operation takes over the battery charge current regulation since the available system peak power cannot deliver enough current to charge the battery at the 50-A current corresponding to the 0.5-V commanding charge-current reference signal. When MPT control is active, the battery current is maximally saturated at 11.35 A, as shown in the bottom plot of Figure 9.

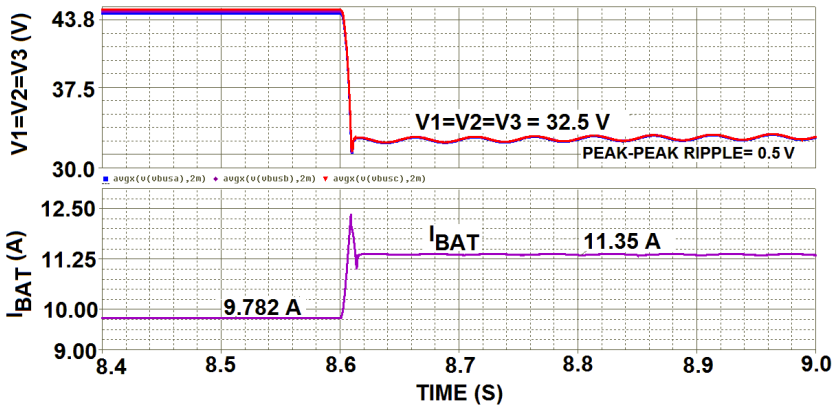

Figure 9 Simulated response of the three-converter DISO power system shown in Figure 2 during a transition from battery-charge current regulation to UIVD input voltage regulation mode of operation

After verifying the basic functionality of the DISO power system shown in Figure 2, the MPT control was extensively simulated. Power sources PS#1, PS#2, and PS#3 have open-circuit voltages of 60 VDC and sourcing resistances of 2.0 Ω, 2.5 Ω, and 2.5 Ω, respectively. To verify UVD control of the three distributed sourcing input voltages, the open-circuit voltages of PS#1 and PS#3 were changed from 60 V to 80 V and 50V, respectively, causing the total sourcing peak power to increase from 1170 W to 1357 W.

The three DISO converters have their outputs connected in parallel across a battery that exhibits very low impedance, so the output current (I_{BUS}) is proportional to the total power delivered by three power sources PS#1, PS#2, and PS#3. A delta change in the net output current (ΔI_{BUS}) delivered by the three DISO converters always reflects a delta change in the total power delivered by the three power sources (ΔP_{SOURCE}). Superimposing a small *ac* dither voltage onto the uniformly controlled converter input voltage (ΔV_1) results in an *ac* bus current signal (ΔI_{BUS}) having three major phase responses: (1) ΔI_{BUS} and ΔV_1 are in-phase when the DC operating voltage across the distributed converter input (V1) is below the peak-power voltage; (2) ΔI_{BUS} and ΔV_1 are 180° out of phase when V1 has its DC voltage above the peak-power voltage; and (3) ΔI_{BUS} and ΔV_1 are 90° out of phase when V1 is at the peak-power voltage. The phase response between these two signals provides the basis for developing the MPT controllers depicted in Figures 3 and 7. The MPT controller compares the two *ac* signals, ΔV_1 and ΔI_{BUS}, and slowly updates the set-point reference voltage, V_{SP}. V_{SP} commands the input voltage regulator to exert a control voltage (V_C) that regulates the distributed-input voltage, V1, at the system peak power voltage.

The dither-signal frequency is low enough to allow the IVR controller to accomplish two functions: (1) regulate the DC component of V1 to be proportional to the commanding set-point voltage (V_{SP}); and (2) track the *ac* ripple voltage (*v*1) to the injected *ac* dither-signal. In this manner, the controlled *ac* ripple voltage superimposed on V1 is always in phase with the dither signal. Consequently, the MPT controller that constantly updates the *dc* component of the set-point voltage (V_{SP}) only needs one feedback signal, the total battery bus current (I_{BUS}). In practice, there is no need to feed the distributed input voltage (V1) as an input signal to the MPT controller since the built-in dither-signal already contains the AC ripple voltage superimposed on V1. Figure 7 also includes the simplified controller, being referred as streamlined MPT controller that processes two signals, I_{BUS} and V_{dither}, and delivers one output signal, V_{SPT}, that consists of the slowly updated *dc* component V_{SP} and the AC dither-signal (V_{dither}).

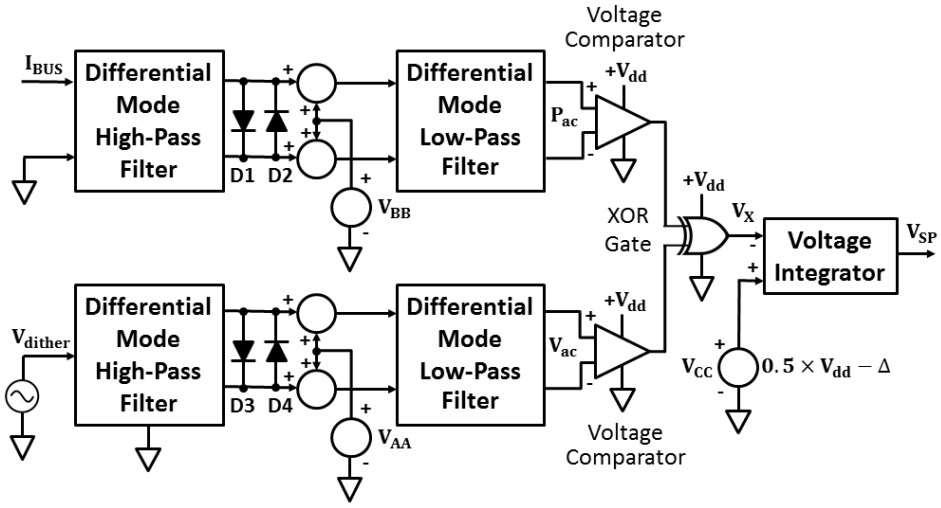

Figure 10 Detailed block diagram of MPT processing circuit previously shown in Figure 8 that needs only one input I_{BUS} and one output V_{SP}

Figure 10 depicts a detailed block diagram of the simpler MPT control block previously shown in Figure 7. The main feedback signal for the MPT processing circuit is the sensed output current (I_{BUS}) of the whole converter power system that is controlled to provide a maximum output current. The front-end differential-mode high-pass filter (HPF) removes the *dc* content from the feedback signal, I_{BUS}, and provides a differential-mode *ac* output signal across the voltage-limiting diodes D1 and D2. The high-pass-filtered *ac* current signal is then low-pass filtered (LPF) and biased with a common-mode voltage to remove high-frequency noise. In this manner, the cascaded differential-mode HPF and LPF stages produce the band-limited *ac* power signal (P_{ac}) that is proportional to the incremental power delivered by the solar array source. Subsequently, a voltage comparator circuit converts P_{ac} into a logical voltage signal. A parallel path of the differential-mode HPF and LPF stages extracts the *ac* signal, V_{ac}, from the dither signal, V_{dither}, that is also converted into another logical voltage signal through a voltage comparator circuit. The filtered dither signal (V_{ac}) is in phase with the solar array dither voltage. Both incremental power P_{ac} and AC dither voltage (V_{ac}) signals are processed through an exclusive-OR (XOR) gate to decode their phase relationship, V_x. Depending on the phase shift between P_{ac} and V_{ac} signals, the *dc* value of the V_x signal will drift from its idle *dc* value, usually set to 50% of the supplying voltage to the XOR gate. The deviation of Vx's average voltage from its idle *dc* value causes the downstream voltage integrator circuit to slowly update its set-point voltage output, V_{SP}, toward a value corresponding to the peak-power voltage of the solar array, V_{mp}. To ensure a proper idle state of the MPT processing circuit, the reference voltage feeding the positive input of the voltage integrator may be slightly reduced by a small value (Δ) such that the idle state of the set-point voltage, V_{SP}, corresponds to the array voltage just below the array peak-power voltage. In this manner, the streamlined MPT controller may stay in an idle state and be triggered for active maximum power tracking as soon as the sensed solar array voltage reduces to the idle set-point voltage of V_{SPMIN}.

When the DISO converter power system is controlled under MPT mode of operation, the transient response of the distributed sourcing input voltage V1 was simulated to verify its stable transition during two simultaneous step changes of the PS#1 open-circuit voltage from 60 V to 80 V and the PS#3 open-circuit voltage from 60 V to 50 V at time t = 5 s. Shown in the middle plot of Figure 11, the three operating sourcing voltages, V1, V2, and V3, are 31V before t = 5 s and 32.23 V after t = 8.5 s, revealing that they respectively are nearly the same as the ideal peak-power voltages of 30 V and 32.04 V. Therefore, the system MPT controller effectively tracks the group peak power using the UIVD approach. As a consequence, the battery charge current increases from 9.8 A to 11.39 A, as shown in the bottom plot of Figure 11, revealing a power increase of 136.8 W that is absorbed by the 90-V battery. As compared to theoretical P-V characteristics, the two tracked peak powers of 1.16 kW and 1.35 kW shown in the top plot of Figure 11 are respectively at 99.1 % and 99.5 % tracking efficiency.

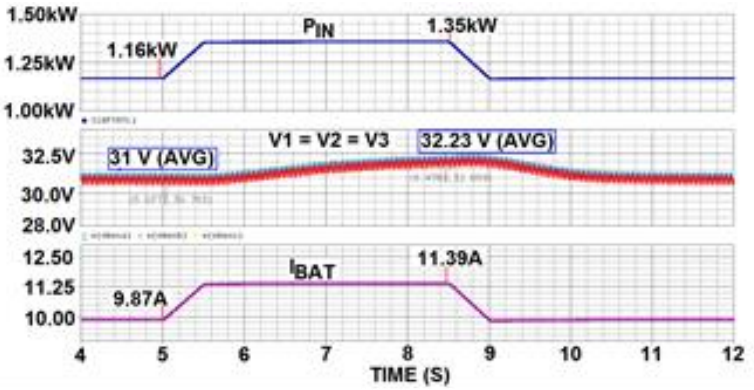

Figure 11 Simulated peak-power voltages of the power system shown in Figure 2 with single-MPT control during simultaneous changes in open-circuit voltages of two sources: one change in power source PS#1 from 60 to 80 VDC and another in power source PS#3 from 60 to 50 VDC

3.2 Simulation of regulated-bus power system with fault-tolerance

For the same power system shown in Figure 6, Figure 12 discloses simulation result of the distributed source voltages on the bottom plot, the system output voltage on the middle plot, and total sourcing power on the top plot, demonstrating the system tolerance of more than one power source failures.

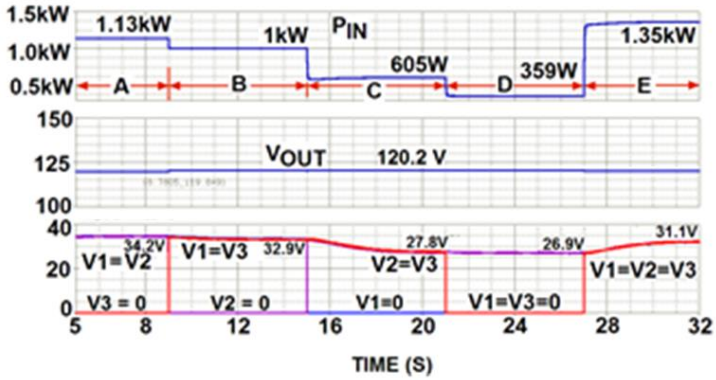

Figure 12 Simulated response of the distributed source voltages, system output voltage, and total sourcing power of the same power system shown in Figure 6 with UIVD-MPT control before, during, and after (1) only one power source failure at a time from t = 9 to 21 s, and (2) two power source failures in tandem (PS#1 and PS#3) from t = 21 to 27 s

For time $5 \leq t < 9$ s, power source PS#3 fails to deliver power (V3=0), and the two remaining power sources are able to deliver their total sourcing power of 1137 W, resulting in 99.9% of tracking efficiency for power sources PS#1 and PS#2. For time $9 \leq t < 15$ s, power source PS#2 fails (V2=0), and the two other power sources are able to deliver 1 kW as their total optimum power, revealing 99.7% of tracking efficiency for power sources PS#1 and PS#3. For time $15 \leq t < 21$ s, power source PS#1 fails (V1=0), and 605 W of the total optimum power is produced from power sources PS#2 and PS#3, demonstrating 99.98 % tracking efficiency. For time $21 \leq t < 27$ s, two power sources, PS #1 and #3, fail and only power source PS#2 delivers its optimum power of 359 W, which is almost the same as the 360-W ideal peak power that PS #2 can offer. As all three power sources are restored to normal after time t = 27 s, they resume 1357 W of the total optimum power. During all of these five simulated scenarios, the system output voltage (the middle plot of Figure 12) is still well regulated at 120 V, and the voltages across any remaining functioning power sources are uniformly distributed as anticipated.

Figure 13 shows the simulated P-V trajectory of power versus total sourcing voltage as shown in red. The simulated P-V response is overlaid on five static P-V characteristics (in purple) having five different peak powers. All the simulation results shown in Figure 12 are extracted from the same PSPICE data file from which the simulated time-domain response is produced, as shown in Figure 12. Regardless of how many power sources experiencing short-circuit across their sourcing terminals; i.e. a single short-circuit fault or two short-circuit faults or no short-circuit fault, the single MPT control with UIVD is able to achieve over 99 % of tracking efficiency for all five optimum power points (points A, B, C, D, and E).

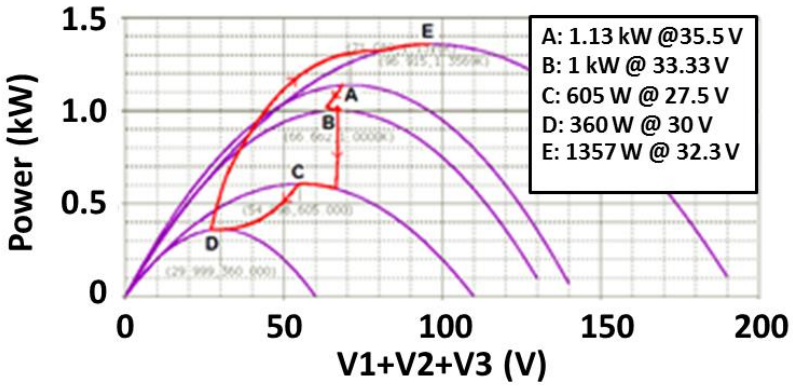

Figure 13 Simulated P-V trajectory of the total sourcing power as a function of the total sourcing voltage as shown in red, for the power system shown in Figure 6 with single-MPT control; the trajectory is overlaid on five static P-V characteristics showing five operating optimum power points: A, B, C, D, and E

Simulation results shown in Figures 12 and 13 are based on the following open-circuit voltages, V_{S1}= 80 V, V_{S2}= 60 V, V_{S3} = 50 V, and the following sourcing resistances, R_{S1} = 2 Ω, R_{S2} = 2.5 Ω, and R_{S3} = 2.5 Ω of the three power sources PS#1, PS#2, and PS#3, respectively.

4. Prototype development and testing

4.1 Description of DISO power prototype

A 3-channel DISO converter power system prototype was built according to the system block diagram shown in Figure 14, revealing only five feedback signals that serve as the inputs to the system controllers. Three sourcing voltages V1, V2, and V3 remain as the basic feedback signals for the system controller to properly distribute three control signal outputs V_{C1}, V_{C2}, and V_{C3} for equal sourcing voltages. The system output voltage of the DISO converters, V_{OUT}, is fed back to the controller so that V_{OUT} is regulated under normal operating conditions, which are considered to be in a non-maximum power tracking (non-MPT) mode. The fifth feedback input is the total sourcing current signal, I_S, which serves as a mandatory signal for computation of the total sourcing power signal. The prototype was developed using a non-isolated input-series connection to the DISO converters of which the distributed sourcing voltages are also a direct contributor of the system output voltage. Three paralleled paths of distributed sourcing voltages are connected in series with the output voltage string consisting of three series-connected outputs of the DISO converters. Three paralleled-cathode diodes CR1, CR2, and CR3 provide a common sourcing voltage V_{RTN} that collects three currents drawn from the three distributed power sources having distributed sourcing voltages V1, V2, and V3, respectively connected to anodes of these diodes. As a result, the system output voltage V_{OUT} consists of four series-connected voltages: V_{O1}, V_{O2}, and V_{O3} which are the output voltages obtained from the three DISO converters, and V_{RTN} which is the common sourcing voltage. System controller still operates in the same manner as that described in section 3. The internal block diagram of the system controller that provides all essential control functions for proper operation of the DISO converter power prototype is given in Figure 15.

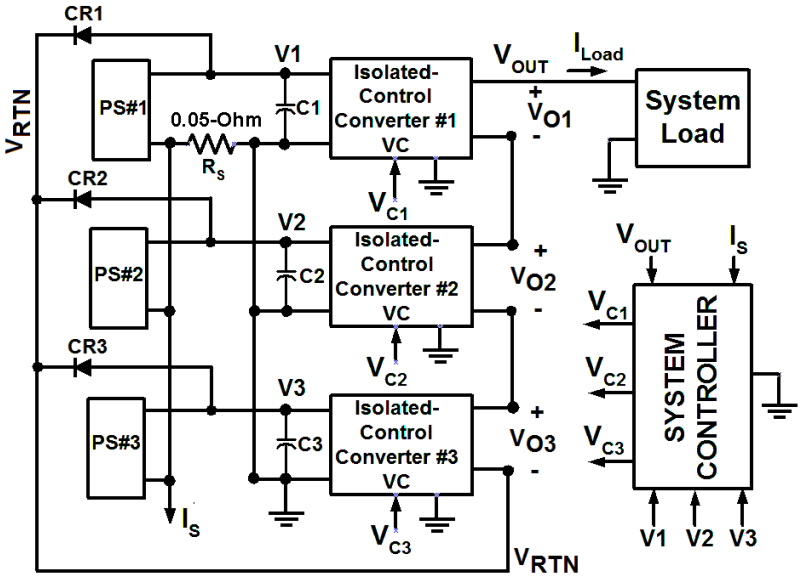

Figure 14 Block diagram of the 3-channel DIPO converter power system including system controller

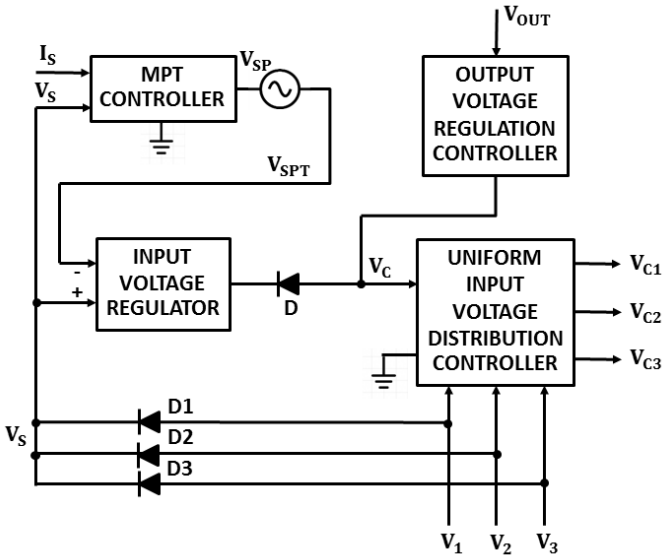

Figure 15 Block diagram of the system controller developed for the prototype shown in Figure 14

Four basic control functions are implemented in the power system prototype: (1) output voltage regulation (OVR), (2) identification of a maximum-power voltage candidate through the MPT controller, (3) input voltage regulation (IVR), and (4) uniform input voltage distribution (UIVD). Under a non-MPT mode of operation, the OVR controller actively regulates the system output voltage V_{OUT} by properly delivering a primary control signal V_C while the MPT and IVR controllers are in their stand-by mode, which does not interfere with the normal OVR function. Diode D shown in Figure 15 is reverse-biased to prevent the IVR control from being in conflict with the output voltage regulation since the sourcing voltages under normal OVR mode are above the minimum sourcing voltage corresponding to the stand-by minimum set-point voltage $V_{SP\text{-}MIN}$ or idle $V_{SP} = V_{SP\text{-}MIN}$. Whenever the

load demand across V_{OUT} exceeds the system maximum power, the OVR controller loses its active regulation, and the sourcing voltages collapse toward the idle minimum sourcing voltage. The sourcing-voltage collapse triggers the MPT and IVR controllers to engage their control contribution to the primary control signal V_C since diode D becomes forward-biased. In this manner, the forward-biased diode D provides an active pull-down to the system control voltage V_C that is no longer controlled by the OVR controller since the output impedance of the IVR controller becomes significantly less than the output impedance of the OVR controller. When this transition from OVR mode to MPT mode occurs, the set-point voltage V_{SP} starts increasing from its minimum idle voltage $V_{SP\_MIN,}$ which corresponds to the minimum sourcing voltage. Consequently, the maximum-limit sourcing voltage V_S is regulated by the IVR controller to track a voltage value corresponding to V_{SP}. Usually, the maximum-limit sourcing voltage V_S is obtained from the strongest power source among the three distributed power sources through the maximum-limit detection circuit, consisting of three paralleled-cathode diodes D1, D2, and D3. Furthermore, V_S also possesses a low-frequency *ac* signal content that is in phase with the *ac* dither signal being superimposed on the maximum-power set-point voltage V_{SP}.

The uniform input voltage distribution controller has sufficient gain and control bandwidth such that the sourcing voltages belonging to weak power sources can be regulated to track the sourcing voltage belonging to the strongest power source. According to the UIVD control block diagram shown in Figures 4 and 5, the UIVD controller still functions properly even with the presence of a short-circuit fault across any power source because voltages across the remaining functional power sources are controllable to be uniformly distributed or nearly equal. In this manner, the 3-channel power system prototype can tolerate failures in up to two power sources.

4.2 DISO power prototype test result

Figure 16 shows the power system response obtained from the prototype when the MPT control is disabled. The three inputs of the power system prototype are supplied by three distributed power sources PS#1, PS#2, and PS#3 having open-circuit voltages of 68.18 V, 57.56 V, and 63.6 V, and their sourcing resistances of 10 Ω, 4 Ω, and 10 Ω, respectively. Shown in the figure are the oscilloscope waveforms of the system output voltage V_{OUT} (green trace), sourcing input voltages V1, V2, and V3 (dark and light blue traces), and the load current I_{LOAD} (red trace) drawn from the system output. During light load current of 1.52 A, V_{OUT} is regulated at 76 VDC, delivering 115 W of output power and uniform sourcing voltages of 54.7 V. When load current increases to 3.68 A under a 14.2-Ω resistive load, V_{OUT} loses its regulation and settles at 52.3 VDC whereas the sourcing voltages are collapsed to a low voltage of 18.3 VDC, signifying poor energy harvesting from the distributed power sources.

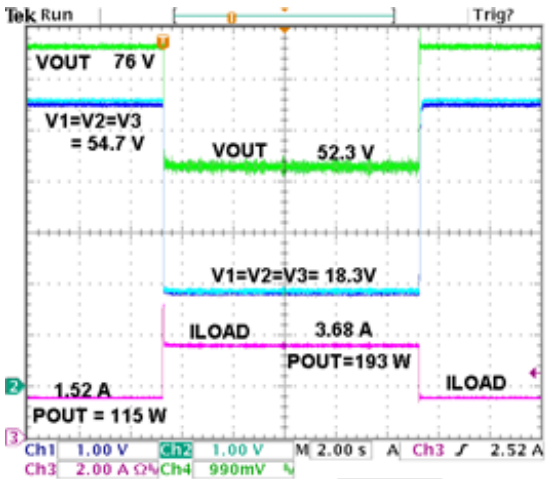

Figure 16 Prototype response when MPT control is disabled

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Figure 17 shows the power system response obtained from the prototype when the MPT control is enabled. The three inputs of the power system prototype are supplied by the same three distributed power sources PS#1, PS#2, and PS#3 having the same open-circuit voltages, and the same sourcing resistances as described earlier for Figure 16. Shown in Figure 17 are the comparable oscilloscope waveforms of the system output voltage V_{OUT} (green trace), sourcing input voltages V1, V2, and V3 (dark and light blue traces), and the load current I_{LOAD} (red trace) drawn from the system output. During 1.52 A of light load current (50-Ω load), V_{OUT} is still regulated at 76 VDC, delivering 115 W of output power and uniform sourcing voltages of 53 V. When load resistance decreases from 50 Ω to14.2 Ω, V_{OUT} loses its regulation and settles at 61.1 VDC which is higher than that (52.3 V) obtained under the non-active MPT control. The sourcing voltages are less reduced to 32.25 VDC and the prototype output delivers 4.29 A load current or 262.1 W of the improved output power from the same power system prototype as a result of active MPT control.

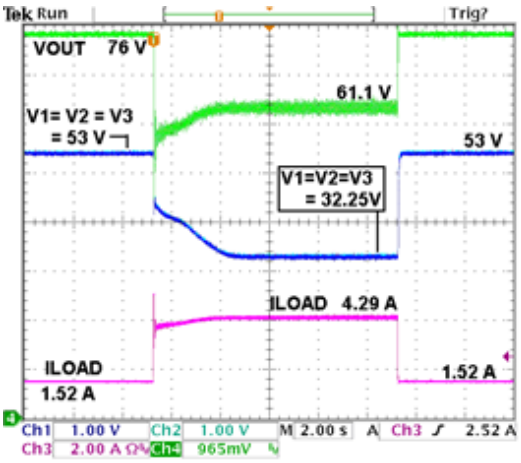

Figure 17 Prototype response when MPT control is enabled

4.3 Testing result of fault-tolerance

The DISO power prototype was also tested to verify its N-1 fault tolerance capability that the system still maintains its maximum power tracking even only one power source is active. To verify effective MPT control with one active power source, MPT function was also disabled for some time so that a collapse of sourcing voltage of the active power source was recognized to be significantly below an optimum sourcing voltage that occurred when MPT function was enabled.

Figure 18 shows the prototype response when each of three power sources is sequentially turned on to increase the system power throughput. Under no load condition and disabled MPT control, the prototype system output voltage is regulated at 76 V and the active sourcing voltage across prototype's channel #1 input is 72 V (V1 in light blue trace) while the two other power sources, PS#2 and PS#3, are inactive. Later, a 15-Ω load is applied across the prototype output while MPT control is disabled, leading to 1.91-A load current (I_{LOAD} in pink trace) that produces 54.6-W output power and a collapse of the PS#1 sourcing voltage to 16.6 V. Subsequently, MPT control is enabled while only PS#1 is active under the same resistive load, causing the PS#1 sourcing voltage to increase to 39 V and the increased output power of 115 W (2.77-A load current). Later, PS#2 is turned on (V2 in green trace) while PS#1 is still active, providing the increased power of 220W (3.83-A load current) and the two equal sourcing voltages of 37.5V (V1 = V2). Finally, PS #3 is turned on as shown in the dark blue trace while PS#1 and PS#2 are active, resulting in a further increase of output power to 320 W (4.62-A load current) and three uniform sourcing voltages of 31.2 V (V1 =V2 =V3).

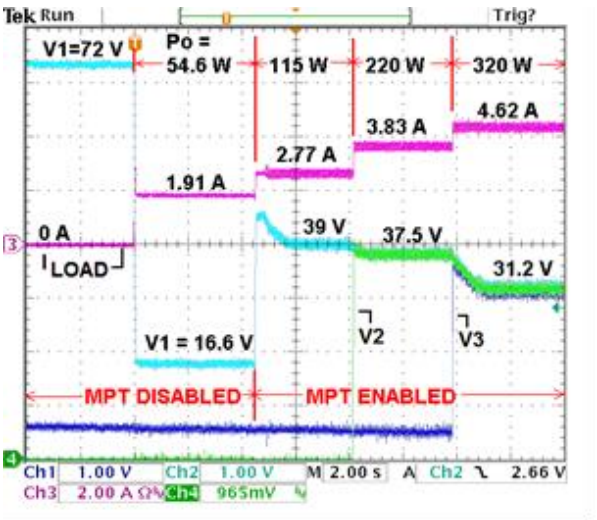

Figure 18 Prototype response when one, two, or three power sources are sequentially turned on for serving as power providers

Figure 19 shows the prototype response when each of three power sources is sequentially turned off to decrease the system power throughput. Under no load condition and enabled MPT control, the prototype system output voltage is regulated at 76 V and the PS#1 and PS#3 sourcing voltages are 72 V (V1 = V3 = 72 V in light blue and green traces) while sourcing voltage of PS#2 is 60 V (V2 in dark blue trace). Later, a 15-Ω load is applied across the prototype output while MPT control is still enabled, leading to 4.62-A load current (in pink trace) that produces 320-W output power and optimally equal sourcing voltages of 31.2 V (V1 = V2 = V3). Subsequently, PS#2 is turned off while MPT control is active under the same resistive load, causing the PS#1 and PS#3 sourcing voltages to increase to 37.5 V (V1 = V3) and the decreased output power of 220 W (3.83-A load current). Later, PS#3 is turned off (in green trace) while PS#1 is still active, providing the increased output power of 115 W (2.77-A load current) and 36.5 V of the PS#1 sourcing voltage. Finally, MPT control is disabled while PS#1 is active, resulting in a further decrease of output power to 54.6 W (1.91-A load current) and the collapsed sourcing of PS#1 to 16.6V.

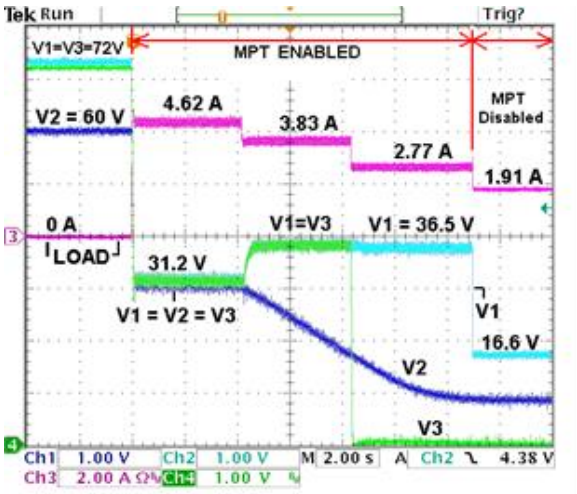

Figure 19 Prototype response when power sources #2 and #3 are sequentially turned off one at a time until only power source #1 is left as a provider

5. Conclusion

Through both PSPICE simulation and prototype testing, the concept of group maximum power tracking for DISO converter architectures has been validated based on uniform input voltage distribution control. With uniform input voltage distribution control, the power delivered by the simulated power system was nearly identical to the available peak power ideally harvestable from the distributed sources. The presented power and control architecture uses a single MPT controller for all input power sources instead of dedicated MPT controllers for each input power source. Such an approach offers near-ideal MPT tracking at reduced system complexity and increased fault tolerance. Provided that the maximum power point voltages of the input power sources are similar, the resulting system architecture offers near-maximum power transfer with a lower parts count despite non-identical power ratings among the power sources.

6. Acknowledgement

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