Optimum power tracking among series-connected power sources with uniform voltage distribution

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Abstract

This paper presents a power system architecture where series-input parallel-output (SIPO) converters are controlled to achieve uniform input voltages across their respective series-connected power sources while also tracking the system optimum power point; the system optimum power point is the maximum power drawn from the series-connected power sources while their voltages are kept uniformly distributed. With proper uniform input voltage distribution control, near maximum use of the power sources is achieved by employing only one maximum power tracking (MPT) controller instead of multiple MPT controllers dedicated for their respective power sources. Provided that the maximum power point voltages of the input power sources are similar, the resulting system architecture offers near-maximum power transfer with a lower parts count. A feasibility study using computer simulation has successfully validated two SIPO power architectures and their control concepts for optimum power transfer.

Keywords**:** *optimum power tracking, uniform voltage distribution, series-connected sources, DC-DC converter, solar array*

1. Introduction

Previous studies (Siri, Conner, & Truong 2005; Siri et al., 2006; Siri & Willhoff, 2007; Siri, Willhoff & Conner, 2007) of SIPO converter architectures employ uniform voltage distribution (UVD) control of the series-connected converter-input voltages for achieving uniform power sharing among the series-connected converters that absorb identical DC input currents drawn from a common power source. This paper proposes slightly different SIPO converter architectures employing UVD control of converter-input voltages to support optimum power flows from the series-connected power sources, each of which is connected across its respective converter's input. For non-identical series-connected power sources, the controller emphasizes optimum power transfer from the series-connected power sources over uniform power sharing among SIPO converters.

Economical and efficient DC power transmission requires high voltage for reduced weight and size of transmission cables before a down-conversion to a low voltage that is usable at a load end. Lack of reliable and expandable power converter architectures and control approaches prohibits efficient transmission and conversion of DC power from a high-voltage input power source (1000 VDC) to a usable low voltage (5 VDC or less) that is increasingly in high demand in both computer-oriented applications and power management for series-connected solar array panels and new battery technologies. SIPO converter power systems have started becoming a viable choice (Siri et al., 2006) for achieving such a high voltage ratio between the system input and output voltages. Feasible UVD control was demonstrated at a medium input voltage range between 108 V and 216 V and a typical output voltage of 28 V (Siri et al., 2006). This paper offers a similar control and power architecture, but focuses on achieving an optimum power throughput and a high output voltage. A controller for series-input parallel-output converter architectures had never been studied to deal with series-connected power sources because of the complexity of the control scheme and difficulties in interfacing the distributed control signals among the series-connected converters. This paper demonstrates that nearly full use of all series-connected sources is achievable by employing uniform input voltage distribution (UIVD) control for two SIPO power architectures. One architecture provides a battery-dominated bus, and another provides a regulated bus serving as the system output. With UIVD control, optimum power use of the series-connected power sources is

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accomplished by using only one maximum power tracking (MPT) controller instead of independent MPT controllers dedicated to each respective power source.

2. Three energy harvesting approaches

Series connection of power sources, such as multiple solar array panels, becomes necessary for cost reductions in DC power transmission over long distances. There exist at least three possible approaches for drawing power from series-connected power sources: (1) directly across the series-connected power sources as group-tracking without uniform voltage distribution control (GT-NO-UVD) of the source output voltage, (2) directly across the series-connected power sources with uniform voltage distribution (GT-UVD) control of their sourcing voltages, and (3) directly across the individual power sources, with each power source possessing its own independent maximum power tracking (IMPT). The IMPT control enables the ideal peak power to be obtainable as a summation of all available peak powers being extracted from all the power sources in the system.

Figure 1 shows the two-terminal GT-NO-UVD approach. The GT-NO-UVD approach results in far-from-optimum utilization of the series-connected power sources, particularly when these sources possess non-identical I-V characteristics. The delivered peak power from the GT-NO-UVD approach is clearly below the ideal available peak power since at least one weak source may become a power dissipater instead of a power provider. Weak solar panels may include a bypass diode across their two sourcing terminals to clamp their negative voltage to a minimum. However, power delivery can still fall significantly below the available peak power.

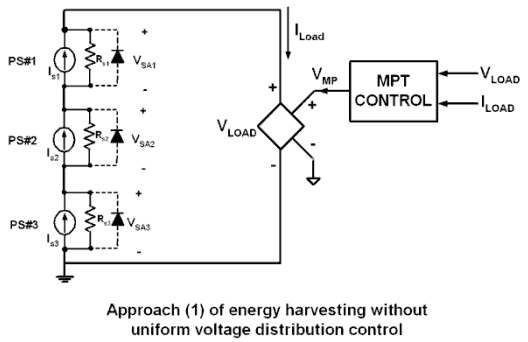

Figure 1 Conceptual system diagram for energy harvesting approach (1) without UVD (GT-NO-UVD)

As depicted in Figure 2, the GT-UVD approach employs distributed DC-DC converters, which are individually connected across their respective power sources to regulate their sourcing voltages providing uniform distribution at all times. In most cases, the GT-UVD approach allows much higher delivered peak power when compared to that obtained by the GT-NO-UVD approach. When the maximum power point voltages of the sources are similar, uniform distribution of the power source voltage ensures that they all become power providers.

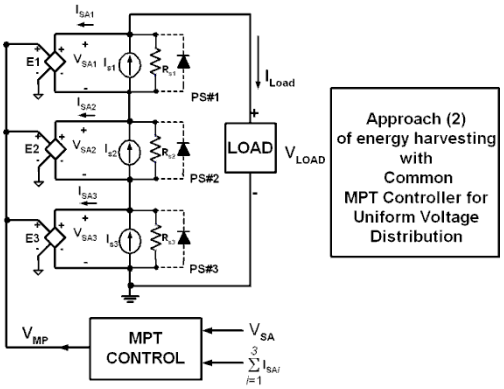

Figure 2 Conceptual system diagram for energy harvesting approach (2) with GT-UVD control

For cases having input power sources with similar peak power voltages, the power delivered by the GT-UVD system approaches the ideal peak power obtained by the IMPT approach shown in Figure 3. However, the series-connected power sources with the GT-UVD approach of energy harvesting can deliver an optimum peak power by employing only one MPT controller. The resulting system architecture offers near-maximum power transfer with reduced complexity and component count.

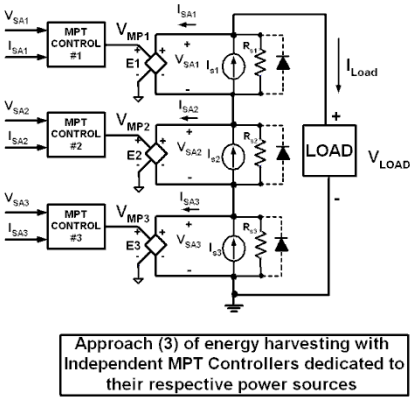

Figure 3 Conceptual system diagram of energy harvesting approach (3) using independent MPT controllers (IMPT)

Figure 4 shows the delivered power as a function of the total sourcing voltage that is the summation of all series-voltages across the individual power sources. The three energy-harvesting methods as shown in Figures 1, 2, and 3 are analyzed through computer simulation using I_{S1} = 6 A, I_{S2} = 21.67 A, and I_{S3} = 20 A with R_{S1} = 10 Ω, R_{S2} = 3 Ω, and R_{S3} = 4 Ω, respectively, representing the three power sources PS#1, PS#2, and PS#3. There are four curves shown in Figure 4: (1) IMPT, (2) GT-UVD, (3) GT-NO-UVD (WITH_BYPASS), and (4) GT-NO-UVD (NO_BYPASS). The curve labeled "IMPT" shown in Figure 4 provides the delivered power when IMPT controllers are distributed to their respective power sources of the configuration shown in Figure 3. The "IMPT" power curve offers the highest peak power that is achievable at 841.6W at the total sourcing voltage of 100.1 V. The delivered power of 831.1W shown in the curve labeled "GT_UVD" is obtained by the UVD controller that actively regulates all the three source voltages to be identical under the conceptual configuration shown in Figure 2. As an example, the peak power delivered by the "GT_UVD" curve is only 1.23% off from the ideal peak power obtained by the IMPT control. Therefore, the Group-Tracking Uniform Voltage Distribution (GT_UVD) system delivers 98.77% tracking efficiency. The delivered power obtained from the remaining two curves labeled "GT_NO_UVD" is accomplished by the group-track without uniform voltage distribution approach. The upper curve labeled as "GT_NO_UVD (WITH_BYPASS)" is obtained from the three non-identical power sources of the configuration shown in Figure 1 with their respective by-passing diodes. The three non-identical and non-ideal power sources equivalently represent three solar array panels that are exposed to different solar illuminations, i.e., due to non-uniform shading or different array-tilting angles facing the sun. The lower curve labeled as "GT_NO_UVD (NO_BYPASS)" is from the same three power sources of the configuration shown in Figure 1 but without the by-passing diodes.

The GT-UVD control for series-connected power sources enables an economical and simple energy harvesting method through the use of a single MPT controller that can be managed to blend with the existing power and control architectures whether their system outputs are regulated-voltage buses or battery-dominated buses.

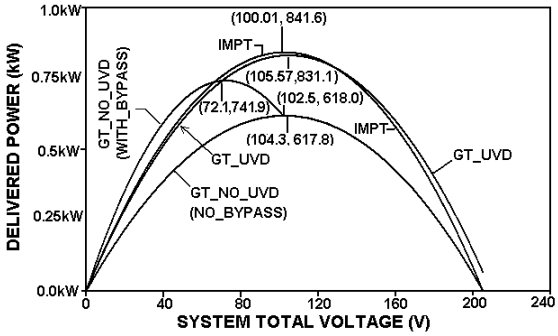

Figure 4 Total delivered power as a function of the total series-connected voltage, showing nearly the same peak-power tracking performance obtained from two optimized control approaches. One is IMPT and the other is the group-tracking approach GT_UVD. The other two group-tracking methods are GT_NO_UVD approaches that deliver much lower peak powers, 741.9 W with by-passing diodes and 617.8 W without by-passing diodes

3. Converter power system description

Figure 5 depicts an output-isolated DC-DC converter with an opto-coupler circuit that provides electrical isolation for controlling the converter power flow using the control input V_{Ci}. In this manner, many isolated-control converters can be series-connected among their input power ports while the converters are independently controllable through their respective control inputs V_{Ci}.

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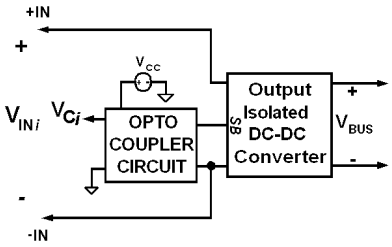

Figure 5 Basic DC-DC converter with an opto-isolated control input V_{Ci} that is electrically isolated from the converter's input power and return terminals

Each isolated DC-DC converter shown in Figure 5 can be a single converter power stage or a group of multiple converter power stages that are connected in parallel. These parallel-connected converter power stages are preferably to a current-mode type. The current-mode converter power stages allow for a common shared-bus voltage signal to command these converter power stages in unison to achieve uniform current-sharing and at the same time to serve other control objectives.

The shared-bus current-sharing among the paralleled current-mode converters was studied (Siri, 1999). Some current-sharing control schemes are not able to employ the commonly controllable current-sharing shared-bus such as the scheme published by Jordan (1999) since the parallel-connected converter power stages are not of the current-mode type

3.1 Battery-dominated power system

Figure 6 illustrates a SIPO converter power system architecture consisting of three input-series-connected converters with their outputs that are parallel-connected across a battery bank having an output voltage V_{BUS}. A system load may be terminated across the output voltage that becomes a battery-dominated voltage bus. Each of these three isolated-control dc-dc converters shares the following attributes: (a) includes a shared-bus control input SB*i*, which allows an external signal to take control of the converter power stage; (b) may represent a number of parallel-connected converter modules configured with shared-bus control inputs tied together to form a common shared-bus control port so as to achieve nearly uniform current-sharing; (c) may operate in a standalone configuration wherein the output is regulated at a pre-determined voltage and its shared-bus input is left unconnected; and (d) must provide electrical isolation between input and output. There are six feedback input signals feeding the system controller shown in Figure 6 : the battery-bus voltage V_{BUS}, the system bus current I_{BUS}, the charging battery-bank current I_{BAT}, and the distributed input voltages V1, V2, and V3 of the series-input connected converters. Figure 7 depicts a conceptual block diagram of the system controller employed in the battery-dominated power architecture shown in Figure 6. The system controller provides four basic control functions: (1) system battery charge control, (2) system series-input voltage regulation, (3) uniform input voltage distribution (UIVD), and (4) system maximum power tracking (MPT). The SIPO converter system may include a bus stabilizer network terminated across the system output V_{BUS} located as close to the system output port as possible to damp out ac energy, thus ensuring system stability.

The controlled voltage on the shared-bus control input SB*i* of each converter must be provided with respect to the input power return of the converter, which is not the same as the common reference ground node of the system controller. The controller usually produces distributed control signals $V_{C1}, V_{C2}, \ldots, V_{CN}$ with respect to the common reference ground. This leads to incompatibility between the distributed control signals and the distributed shared-bus voltages that need to be individually referenced to their respective input power return terminals of the input-series connected converters. Therefore, a proper means of signal-level shifting is needed, such as opto-coupler circuits for properly distributing each of the respective system control voltages to each converter's shared bus input SB*i*, as previously shown in Figure 5.

Typically, the battery charge controller shown in Figure 7 regulates the battery-bank voltage V_{BUS} to a preset value in accordance with its voltage-temperature (V/T) profile to prevent battery over-charging. When the battery-bank voltage V_{BUS} is below its preset value that is pre-assigned as a function of temperature, the battery-bank current I_{BAT} is regulated at a preset charge-current set-point determined by the charge controller. Active battery regulation of either its voltage, V_{BUS}, or charge current, I_{BAT}, leads to a forward-voltage bias across the pull-down diode, D, shown in Figure 7. However, when V_{BUS}'s voltage and I_{BAT}'s current are respectively below the preset voltage value and the preset charge-current set-point, the system controller regulates the system series-input voltage V1 at the peak-power voltage that is determined by the MPT control. As the operating battery-bank voltage and current are below their preset voltage/charge-current values, the power system is instead controlled to have an optimum power transfer from all series-connected power sources by utilizing only one MPT controller that dominates its control over the battery charge controller through the primary control signal V_C and the reverse-biased diode, D. During an active control of either the battery charge current or the series-input voltage, uniform voltage distribution among converter-input voltages delivered by all series-connected power sources are always actively regulated by the UIVD controller. It properly distributes three control voltage signals V_{C1}, V_{C2}, and V_{C3} to their respective isolated-control converters #1, #2, and #3.

In general, a SIPO power system may consist of *N* isolated-control DC-DC converters with their respective *N* series-connected power sources PS#1, PS#2, . . . , PS#*N*. During either the battery voltage/current regulation or the series-input voltage regulation, the converter-input voltage distribution controller produces secondary voltage distribution controller produces secondary control signals ($V_{d1}, V_{d2}, \ldots, V_{dN}$). The secondary control signals are subtracted from the primary control voltage, V_C, to create a modified control

voltage (V_{C1}, V_{C2}, . . . , V_{CN}) that regulates its respective converter to accomplish uniform input voltage distribution. Figure 8 illustrates a potential control block diagram that generates a common distributed reference signal, $V_{DIS} = V_I/N$, as the central-limit (CL) distribution reference, where N=3 is the number of series-connected converters. The voltage difference between V_{DIS} and each converter-input voltage (V_{i1}, V_{i2} , . . . ,V_{iN}) is amplified, frequency-compensated, and finally output as the voltage distribution control signal (V_{d1}, $V_{d2,}$ . . . , and V_{dN}, respectively). Each secondary control signal, V_{di}, provides a minor control correction to the primary control voltage, V_C, thus ensuring uniform input voltage distribution.

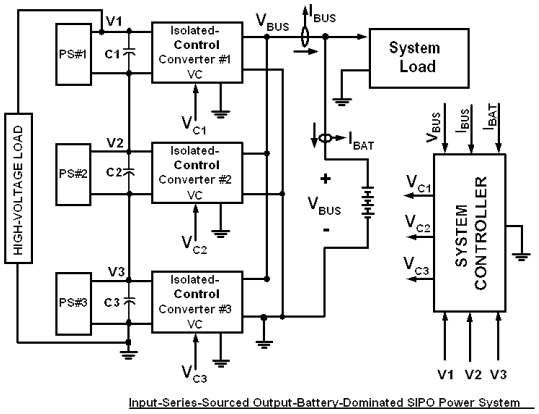

Figure 6 Battery-dominated *3*-converter SIPO power system with 3 series-connected power sources

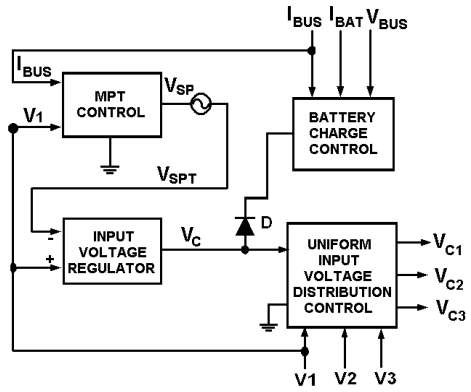

Figure 7 SIPO converter power system UIVD controller

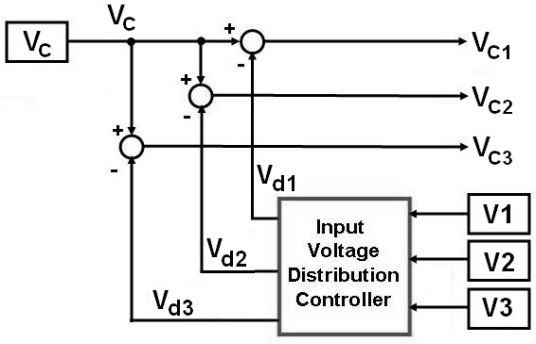

Figure 8 Uniform input voltage distribution controller block diagram for 3 series-connected converters

The UIVD controller shown in Figure 8 is not fault-tolerant when the common distributed reference signal, $V_{DIS} = V_I/N$, is the central-limit (CL) distribution reference. If one converter fails and cannot be controlled due to a short circuit across its input, the system will lose regulation. Figure 9 shows the improved UIVD controller that is based on the Maximum-Limit (ML) distribution reference, V_{DIS} = MAX(V_{i1}, V_{i2} , . . . ,V_{iN}). To achieve fault-tolerance, a set of ideal rectifiers is included as part of the UIVD controller to produce a common distributed voltage reference signal, V_{DIS}, which represents the highest converter-input voltage obtained from one of the converters within the power system. Therefore, if a converter fails with its input short circuited, V_{DIS} is automatically increased to compensate for the loss of a failed converter. For the system to tolerate at least one converter input short-circuit failure, two ideal rectifiers are required to sense the output voltage from any two converters. Up to *N* ideal rectifiers are included in the UIVD controller for an *N*-converter SIPO system.

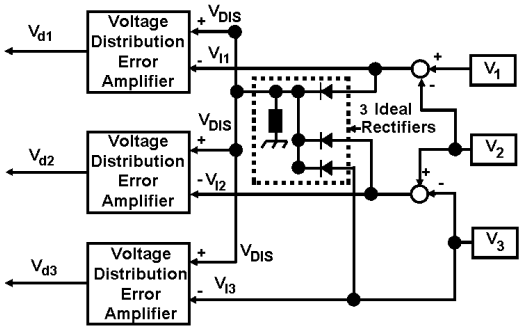

Figure 9 Fault-tolerant uniform input voltage distribution controller using the Maximum-Limit distribution reference

Consequently, Figure 9 illustrates the UIVD control for a three-converter SIPO power system with fault-tolerance. A common distributed voltage reference signal, V_{DIS}, is derived from three cathode-parallel-connected ideal rectifiers so as to individually sense the input voltages of converters #1, #2, and #3. If one converter fails to build up its input voltage, the two remaining converters will be controlled to have uniform input voltage distribution of up to one-half of the system input voltage V1.

The *dc* gain for each voltage distribution error amplifier shown in Figure 9 does not need to be high in order to achieve uniform input voltage distribution. On the contrary, high *dc* gain within each distribution error amplifier causes the converter-input voltage distribution controller to dominate the battery charge control and the series-input voltage regulation modes of operation, resulting in insufficient charging to the battery bank.

3.2 Regulated-bus power system

Figure 10 shows another SIPO converter power system architecture consisting of three input-series-connected converters with their outputs that are parallel-connected across a battery bank having an output voltage V_{BUS}. A system load may be terminated across V_{BUS} output voltage that becomes a battery-dominated voltage bus. Each of these three isolated-control dc-dc converters share the same four attributes as previously described for Figure 6. There are seven feedback input signals feeding the system controller shown in Figure 11: the battery-bus voltage V_{BUS}, the regulated-bus output voltage BUSOUT, the system battery-bus current I_{BUS}, the charging battery-bank current I_{BAT}, and the distributed input voltages V1, V2, and V3 of the series-input connected converters. Figure 11 depicts a conceptual block diagram of the system controller employed in the dual-bus power architecture shown in Figure 10. The system controller provides five basic control functions: (1) system BUSOUT's voltage regulation, (2) system battery charge control, (3) system series-input voltage regulation, (4) uniform input voltage distribution (UIVD), and (5) system maximum power tracking (MPT). In the same manner, a bus stabilizer network may be terminated across the system output BUSOUT located as close to the system output port as possible to damp out AC energy, thus ensuring system stability. The system regulated-bus voltage is closed-loop controlled by an output-isolated DC-DC converter with its output port V_{O4} that is series-connected with the total system input voltage V1. The control signal V_{C4} drives the converter's power stage to regulate the BUSOUT's voltage at a fixed value above the system input voltage V1.

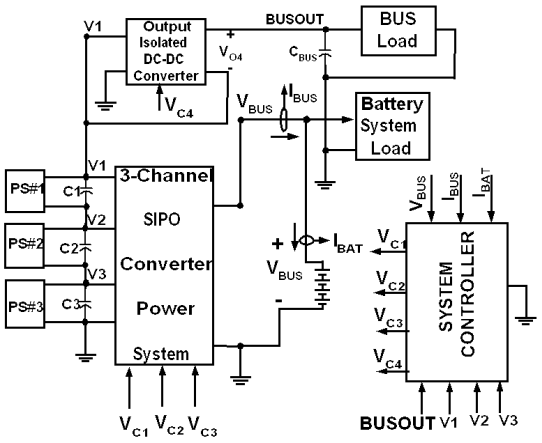

Figure 10 Dual-Regulated Bus Power Architecture with UIVD control

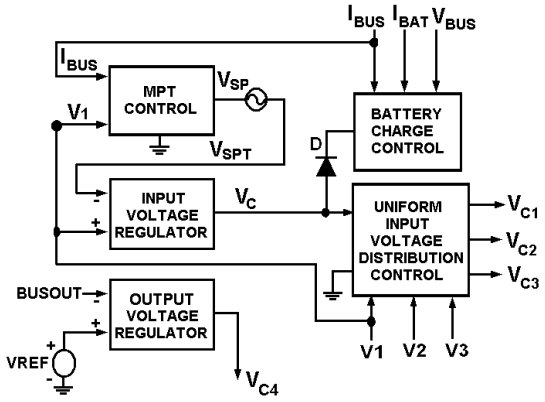

Figure 11 System controller for the dual regulated buses employed in the system shown in Figure 10

4. Simulation of SIPO power systems with uniform voltage distribution

4.1 Battery-dominated power system simulation

A PSPICE model of the battery-dominated bus power system with three SIPO converters and three series-connected power sources, as shown in Figure 6, was developed and simulated to verify the basic functionality of each control loop. In addition, active input-current limiting was also included for limiting the system input current to a pre-determined value. To verify the fundamental control behavior, the MPT control is disabled, and a fixed solar array set-point voltage, V_{SPT}, is instead used to command the

input-voltage regulation control loop to regulate the system input voltage, V1, at 120 VDC.

Figure 12 shows the simulation result that demonstrates a mode transition from the input-voltage regulation mode to the input-current limiting mode in which the current-limiting set-point reference is reduced from far above 11 A to about 9.9 A at time t = 82 ms. This causes the system input current to drop from 11.1 A to 9.9 A (trace with "I(RSENS)" label on the top plot), and the system input voltage V1 to increase from 120 V to 129.6 V (trace with label "V1" on the bottom plot). During both modes of operation in steady state and their transient mode transitions, the three series-connected voltages across the individual inputs of three respective converters are controlled to have uniform distribution at all times, as shown in three overlapping traces on the bottom plot.

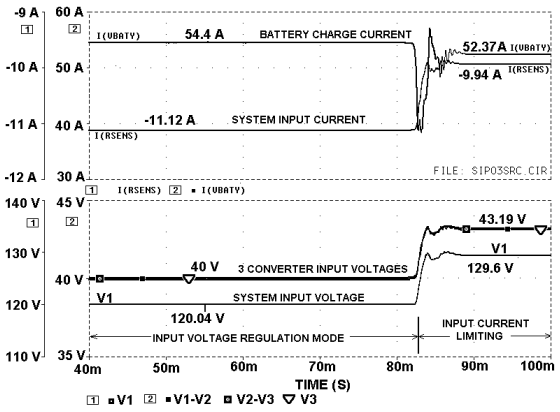

Figure 12 Simulated response of the three-converter SIPO power system shown in Figure. 6 during both input voltage regulation and input current-limiting modes of operation and their transient transition

Figure 13 illustrates another PSPICE simulation result that uncovers a transition from the battery charge current regulation mode to the input current-limiting mode. The current-limiting set-point is reduced from far above 11A to approximately 5 A at time t = 60 ms. As a result, the system input current drops from 9 A to 5 A (trace with "I_{IN}" label on the bottom plot), and the three converter- input voltages, V1-V2, V2-V3, and V3 to increase from 45.5 V to 56.4 V (three overlapping traces on the top plot). During steady-state operation and the transient mode transitions, the three series-connected input voltages are controlled to have uniform distribution at all times, as shown in the three overlapping traces on the top plot of Figure 13.

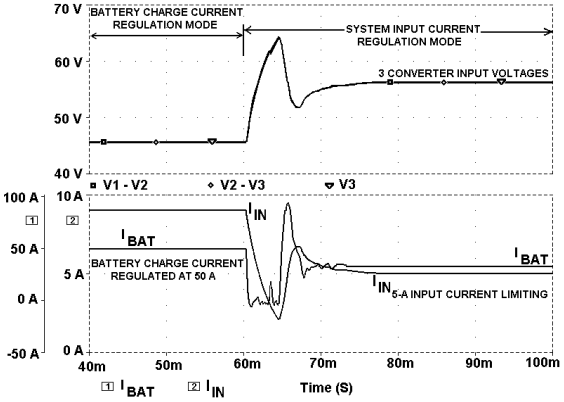

Figure 13 Simulated response of the three-converter SIPO power system shown in Figure. 6 during both battery-charge current regulation and input current-limiting modes of operation and their transient transition

After verifying the basic functionality of the SIPO power system shown in Figure 6, the MPT control was restored and simulated. Power sources PS#1, PS#2, and PS#3 have open-circuit voltages of 50 VDC and sourcing resistances of 2.0Ω, 2.5Ω, and 4.5Ω, respectively. To verify UVD control of the three series-connected input voltages, the open-circuit voltage of PS#3 was changed from 50 V to 80 V, causing its peak power to increase from 701 W to 878 W.

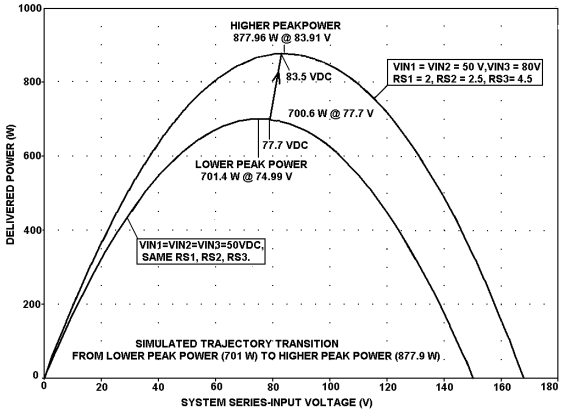

Figure 14 Anticipated response of the SIPO power system, with a single MPT controller, revealing a possible transition from a lower peak power to a higher peak power due to changes in I-V characteristics of one power source among three power sources controlled by three series-connected converters as shown in Figure. 6

Figure 14 depicts the theoretical delivered power as a function of the total sum of the series-connected converter-input voltages under UVD control. When the three sources have identical open-circuit voltages of 50 VDC, the peak-power voltage is 77.7 V, and the total peak power is 701 W, as shown in the lower curve. When the open-circuit voltage of PS#3 is changed to 80 V, the peak-power voltage becomes 83.5 V, and the delivered peak power is 878W, as shown in the upper curve. Therefore, the peak power voltage should change from 77.7 V to 83.5 V with the MPT controller enabled.

The three SIPO converters have their outputs connected in parallel across a battery that exhibits very low impedance, so the output current, I_{BUS}, is proportional to the sum of the three powers delivered by PS#1, PS#2, and PS#3. A delta change in the net output current (ΔI_{BUS}) delivered by the three SIPO converters always reflects a delta change in the total power delivered by the three power sources (ΔP_{SOURCE}). Superimposing a small AC dither voltage onto the uniformly controlled converter input voltage (ΔV_1) results in an AC output current signal (ΔI_{BUS}) having three major phase responses: (1) ΔI_{BUS} and ΔV_1 are in-phase when the DC operating voltage across the three series-connected converter inputs V1 is below the peak-power voltage, (2) ΔI_{BUS} and ΔV_1 are 180° out of phase when V1 has its DC voltage above the peak-power voltage, and (3) ΔI_{BUS} and ΔV_1 are 90° out of phase when V1 is at the peak-power voltage. As shown in Figures 15 through 17, the phase response provides the basis for the developing the MPT controllers depicted in Figure 6 or Figure 10. The MPT controller compares the two AC signals, ΔV_1 and ΔI_{BUS}, and slowly updates the set-point reference voltage, V_{SP}; V_{SP} commands the input voltage regulator to exert a control voltage, V_C, that regulates the system series-input voltage V1 near the peak power voltage.

The dither-signal frequency is low enough (10 Hz for simulated results shown in Figures 15 to 17) to allow the IVR controller to accomplish two functions: (1) regulate the DC component of V1 to be proportional to the commanding set-point voltage V_{SP} and (2) track the AC ripple voltage, $v1$, to the injected AC dither-signal. In this manner, the controlled AC ripple voltage superimposed on V1 is always in phase with the dither signal. Consequently, the MPT controller that constantly updates the DC component of the set-point voltage V_{SP} only needs one feedback signal, the total battery bus current I_{BUS}. In practice, there is no need to feed the series-input voltage V1 as an input signal to the MPT controller since the built-in dither-signal already contains the AC ripple voltage superimposed on V1.

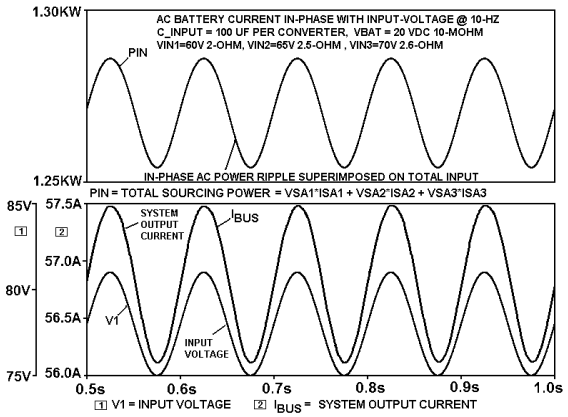

Figure 15 Simulated AC response of the system series-input voltage V1 and the system output current I_{BUS}, with a single MPT controller, revealing an in-phase response of I_{BUS} with respect to the system voltage V1 that has its DC operating point below the peak-power voltage

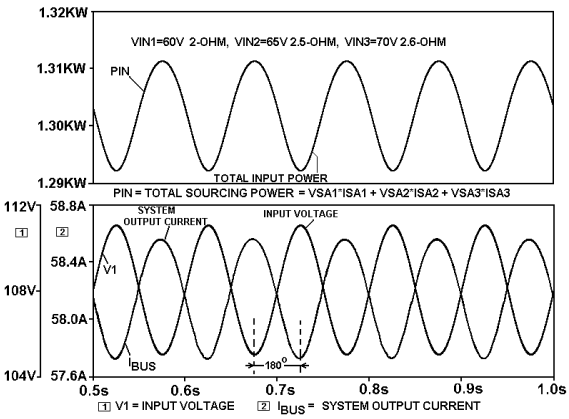

Figure 16 Simulated AC response of the system series-input voltage V1 and the system output current I_{BUS} of the same power system, revealing an out-of-phase response of I_{BUS} with respect to the system voltage V1 that has its DC operating point above the peak-power voltage

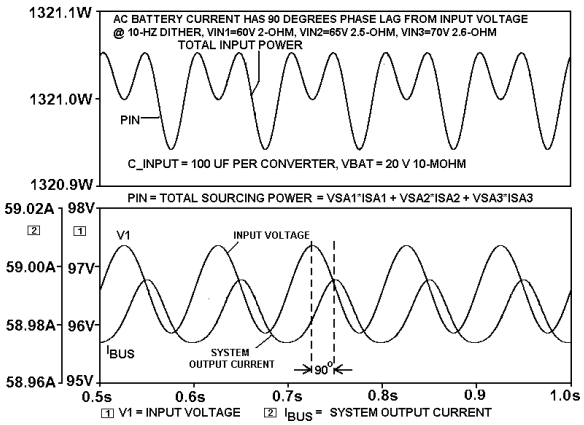

Figure 17 Simulated AC response of the system series-input voltage V1 and the system output current I_{BUS} of the same power system, revealing a 90° out-of-phase response of I_{BUS} with respect to the system voltage V1 that has its DC operating point at the peak-power voltage

Figure 18 shows the simplified controller. The streamlined MPT controller processes two signals, I_{BUS} and V_{dither}, and delivers one output signal, V_{SPT}, that consists of the slowly updated DC component V_{SP} and the AC dither-signal V_{dither}. The streamlined MPT controller is an improved result from simplification of the former MPT controllers developed under previous studies (Siri & Conner, 2001; Siri & Conner, 2002; Siri & Conner, 2003).

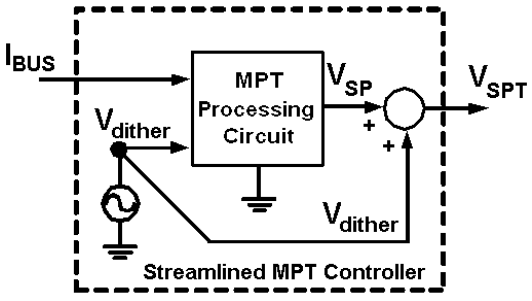

Figure 18 Streamlined MPT controller requiring only one feedback input—the total battery bus current I_{BUS} with no need for the other feedback input V1

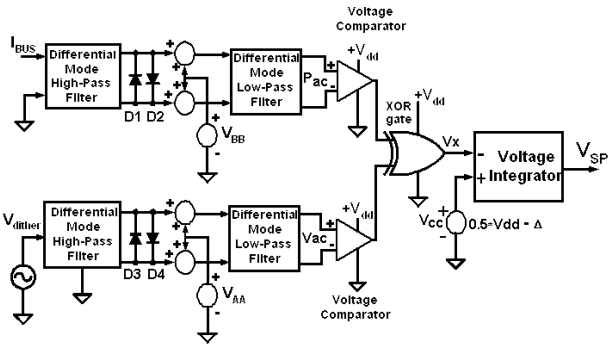

Figure 19 Detailed block diagram of MPT processing circuit previously shown in Figure 18 that needs only one input I_{BUS} and one output V_{SP}

Figure 19 depicts a detailed block diagram of the MPT control block previously shown in Figure 18. The main feedback signal for the MPT processing circuit is the sensed output current, I_{BUS}, of the converter that is controlled to provide a maximum output current. The front-end differential-mode high-pass filter (HPF) removes the DC content from the feedback signal, I_{BUS}, and provides a differential-mode AC output signal across the voltage-limiting diodes D1 and D2. The high-pass-filtered AC current signal is then biased with a common-mode voltage and low-pass filtered (LPF) to remove high-frequency noise. In this manner, the cascaded differential-mode HPF and LPF stages produce the band-limited AC power signal, P_{ac}, that is proportional to the incremental power delivered by the solar array source. Subsequently, a voltage comparator circuit converts P_{ac} into a logical voltage signal. A parallel path of the differential-mode HPF and LPF stages extracts the AC signal, V_{ac}, from the dither signal, V_{dither}, that is also converted into another logical voltage signal through a voltage comparator circuit. The filtered dither signal, V_{ac}, is in-phase with the solar array dither voltage. Both incremental power P_{ac} and AC dither voltage V_{ac} signals are processed through an exclusive-OR (XOR) gate to decode their phase relationship, V_x. Depending on the phase shift between P_{ac} and V_{ac} signals, the DC value of the V_x signal will drift from its idle DC value, usually set to 50% of the supplying voltage to the XOR gate. The deviation of V_x's average voltage from its idle DC value causes the downstream voltage integrator circuit to slowly update its set-point voltage output, V_{SP}, toward a value corresponding to the peak-power voltage of the solar array, V_{mp}. To ensure a proper idle state of the MPT processing circuit, the reference voltage feeding the positive input of the voltage integrator may be slightly reduced by a

small value, Δ, such that the idle state of the set-point voltage, V_{SP}, corresponds to the array voltage just below the array peak-power voltage. In this manner, the streamlined MPT controller may stay in an idle state and be triggered for active maximum power tracking as soon as the sensed solar array voltage reduces to the idle set-point voltage of V_{SPMIN}.

After restoring MPT control to the SIPO power system, the transient response of the system series-input voltage V1 was simulated to verify its stable transition during a step change of the PS#3 open-circuit voltage from 50 V to 80 V at time t = 60 s. As shown in the top plot of Figure 20, the two operating voltages at V1, 78.28 V before t = 60 s and 83.16 V after t = 67 s, are nearly the same as the ideal peak-power voltages of 77.7 V and 83.5 V depicted in Figure 14. Therefore, the system MPT controller effectively tracks the peak power using the UVD approach. During the transient transition, the battery charge current increases from 31.7 A to 39.3 A, as shown in the bottom plot of Figure 20, revealing a power increase of 152.5 W that is absorbed by the 20-V battery.

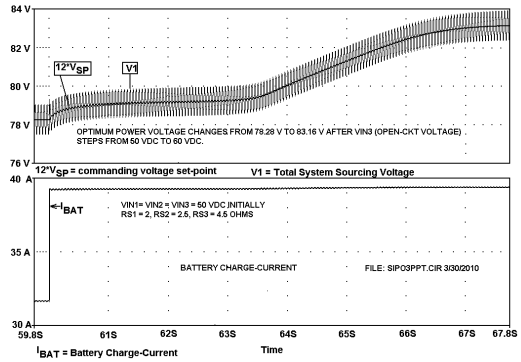

Figure 20 Simulated peak-power voltage response of the power system shown in Figure. 6 with single-MPT control during an increased supplying voltage of power source PS #3 from 50 VDC to 80 VDC

With the same sourcing resistances and open-circuit voltages for the three power sources (PS#1, PS#2, PS#3), the tracked peak-power voltage across V1 and the power ground is verified to be sustainable despite step-load transients across the V1 bus. Figure 21 shows the simulated voltage response at V1 under a transient 3-A step-load at time = 60 s. It takes approximately 4 seconds for the input series-voltage V1 to reach its steady peak-power voltage of 78.2 VDC. The single-MPT controller with UVD tracks the peak-power voltage without loss of system stability. The battery charge current reduces from 31.7 A to 21.1 A to compensate for the increased load across the input series-voltage.

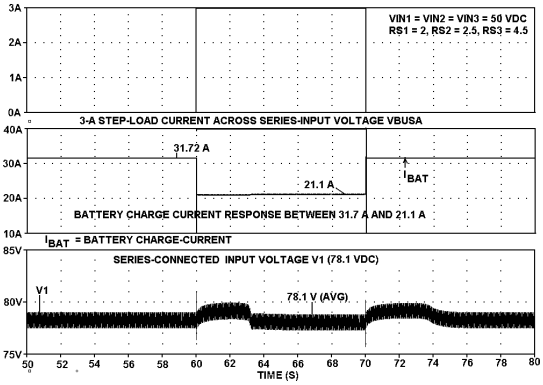

Figure 21 Simulated response of the input series-voltage V1 in the power system shown in Figure. 6 with single-MPT control during a 3-A step load drawn across the V1's input bus

Similarly, Figure 22 shows another simulated voltage response across V1 bus under a step transition to a 600-W constant-power load that occurred at time t = 40 s. Again, it takes about 4 seconds for the input series-voltage V1 to reach its steady peak-power voltage of around 78.2 VDC, confirming that the single-MPT controller with UVD tracks the same group peak-power voltage with robust stability. The battery charge current reduces from 31.7 A to 1.48 A to naturally compensate for the increased load across the input series-voltage.

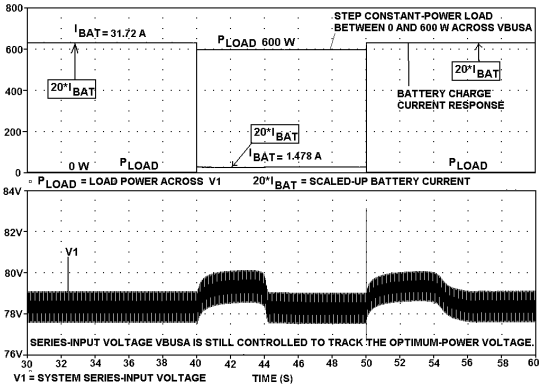

Figure 22 Simulated response of the series-voltage V1 in the same power system with single-MPT control during a step into/out of a 600-W constant-power drawn across the V1's input bus

4.2 Regulated-bus power system simulation

A PSPICE model of the regulated-bus power system with three SIPO converters and three series-connected power sources, as shown in Figure 10, was simulated to verify the basic functionality of its control loops. Bus output voltage regulation was added into the system for regulating the bus voltage (BUSOUT) at 100 VDC. The single-MPT control with UVD ensures the continuously updated solar array set-point voltage, V_{SPT}, that commands the input-voltage regulation control loop to regulate the system input voltage, V1, at the group peak-power voltage of 78.2 VDC.

Figure 23 illustrates the simulated response of the system output bus voltage at node BUSOUT as V(BUSOUT) and the series-input voltage, V1, plotted on the bottom plot. The system output voltage across BUSOUT and ground is well regulated at 110 VDC at all times despite a 5-A step-load that is shown as "$I_{BUSLOAD}$" trace on the top plot. As a consequence of the 5-A step-load, the battery charge current, I_{BAT}, drops from 26.3 A to 6.8 A since the single-MPT controller sustains its tracking of the group peak-power voltage V1 of 78.2 VDC without loss of UVD control.

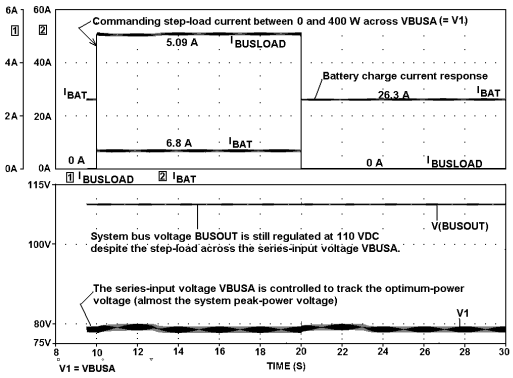

Figure 23 Simulated response of the peak-power voltage V1 and the system output bus voltage BUSOUT for the power system shown in Figure. 10 with single-MPT control during a 5-A step-load current across the series-voltage bus V1

Figure 24 depicts another set of simulated responses of the system output bus voltage BUSOUT, the series-input voltage V1, and the battery charge current as a result of a step-load across the output bus voltage (between BUSOUT and ground). The step-load between 1.1 A and 5.28 A (shown as $10*I_{BUSLOAD}$ trace on the top plot) causes the battery charge current (shown as I_{BAT} trace on the top plot) to correspondingly step between 25.8 A and 2.47 A to maintain the system peak-power voltage V1 at 79.93 V (on the bottom plot). The system output voltage across BUSOUT and ground (the middle plot) is still well regulated at 110 VDC at all times despite the step-load. The BUSOUT's voltage has an AC voltage-ripple content at the same dither frequency used for peak-power tracking. The single-MPT controller, while maintaining the tracking of the peak-power voltage without loss of UVD control, also regulates the AC ripple voltage superimposed on its operating peak-power voltage.

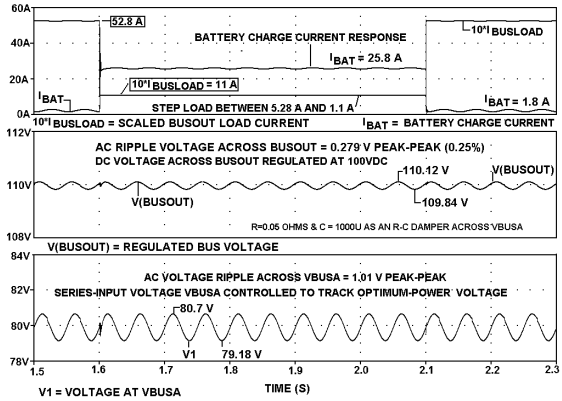

Figure 24 Simulated response of the peak-power voltage V1 and the system output bus voltage BUSOUT for the power system shown in Figure. 10 with single-MPT control during step-load transitions across the regulated bus BUSOUT

5. Conclusion

Computer simulation has validated optimum power tracking for a Series-Input, Parallel-Output converter architecture with uniform input voltage distribution among series-connected power sources. With uniform input voltage distribution control, the power delivered by the simulated power system was nearly identical to the peak power available from the source. However, the presented architecture uses a single MPT controller for all input power sources instead of distributed MPT controllers, each of which is dedicated for each input power source. Such an approach offers near-ideal MPT tracking at reduced system complexity. Provided that the maximum power point voltages of the input power sources are similar, the resulting system architecture offers near-maximum power transfer with a lower parts count.

6. References

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